REMARKS

1. The specification is amended in response to the Examiner's objection. No new matter is added.

2. The abstract of the disclosure is amended in response to the Examiner's objection. A clean abstract is enclosed.

3. Claims 1 and 22 are amended in response to the Examiner's rejection. Claims 18-21 are amended to correct typographical errors. No new matter is added.

4. Claims 12-21 are rejected under 35 U.S.C. 101 as being non-statutory as failing to provide any real world tangible result. The Examiner is respectfully requested to withdraw the rejection of claims 12-21 in view of the following comments.

MPEP 2106 (IV)(C) (2) states "A claimed invention is directed to a practical application of a 35 U.S.C. 101 judicial exception when it … "transforms" an article or physical object to a different state or thing… USPTO personnel first shall review the claim and determine if it provides a transformation or reduction of an article to a different state or thing. If USPTO personnel find such a transformation or reduction, USPTO personnel shall end the inquiry and find that the claim meets the statutory requirement of 35 U.S.C. 101."

Claim 12 recites writing bytes of the first words to two memories and transferring bytes between the two memories, which inherently involve reading bytes out of one memory and writing them to the other. The process of writing data to a memory transforms the memory into a different state. Each physically transformed memory thus comprises a tangible result of the method.

Claim 12 also recites forming a sequence of N-byte second words from a sequence of N-Byte first words wherein each second word comprises bites of more than one of the first words. As discussed below, such a "convolutionally interleaved" word sequence is useful, for example, because when encoded into a transmitted signal it can convey data representing speech that is less subject to distortion due to noise bursts. The Federal Circuit Court in **In Re Allapat** 31 U.S.P.Q. 2d 1545 (CAFC 1994) held that useful data (in that particular case data indicating "a final share price") is "a useful, concrete and tangible result" sufficient to meet the statutory requirement of 35 U.S.C. 101.

This type of claim in which data is produced and written to memory has substantial precedence. Note, for example, that claim 1 of U.S. Patent 6,971,057, which the Examiner not only cited as prior art but also previously examined and correctly found to be permissible under 35 U.S.C 101, also convolutionally interleaves one data sequence to produce another in part by writing data to a memory. The tangible results of that method are also useful data and a physically altered memory. See also claim 1 of each of the following U.S. patents: 6,421,796, 6,151,690, 5,991,857, and 5,745,497, all of which are cited by U.S. Patent 6,971,057.

Thus claim 12 meets the statutory requirement of 35 U.S.C. 101 because it recites writing data to a memory, thereby transforming an article to a different state, and also because it recites forming useful data, which according to the Federal Circuit Court is "a useful, concrete and tangible result". Claims 13-21 meet the statutory requirements of 35 U.S.C. 101 for similar reasons.

5. Claims 1-22 are rejected under 35 U.S.C. 102(e) as being unpatentable over US patent 6,971,057 (Delvaux). The Examiner is

respectfully requested to withdraw this rejection in view of the following comments distinguishing these claims over Delvaux.

Claims 1, 2, 4 - 12, and 14-22

The invention as recited in claim 1 can implement an interleaver as illustrated in FIG. 5. The interleaver receives and stores bytes forming words of an incoming sequence A, and then forms an outgoing sequence B in which the bytes forming words of sequence A have been convolutionally interleaved so each word of sequence B contains bytes of more than one word of sequence A.. The interleaver assembles the next set of words to be forwarded in as sequence B in a cache memory 50.

As each byte of sequence A arrives in a buffer 42, a controller 40 decides whether it is to be included in the next set of words of sequence B, and if so, the controller stores the incoming byte in cache memory 50. The controller also block writes all bytes of sequence A arriving in buffer 42 in a separate main memory 46 whenever the buffer is full. Whenever controller 40 has stored all words of the next set of sequence B words in cache memory 50, it forwards that set of words to an output buffer 52 as sequence B, thereby clearing memory 50. The controller 40 then transfers to cache memory 50 all sequence A bytes stored in main memory 46 that are to be included in a next set of sequence B words to be forwarded. If that next set of sequence B words is not yet complete, it waits until it has stored in cache memory 50 the missing sequence B words as they arrive via sequence A before forwarding that next set of sequence B words from the cache memory.

Memory 46 can be a large, but relatively cheap, RAM assessable by DMA block operations while cache memory 50 must be a relatively fast RAM because it is accessed only on a byte-by-byte basis. If only a single memory were used for storing sequences, it would have to be both large and fast and therefore

much more expensive than using two memories in the manner taught by the application.

Accordingly claim 1 recites an apparatus for forming a sequence of second words from bytes forming a sequence of first words. The apparatus comprises a main memory (46), a cache memory (50) and a control circuit (40) for writing bytes of each first word into either the main memory or the cache memory, for transferring bytes between the main memory and the cache memory, and for forming each second word from bytes stored in the cache memory such that each second word comprises bytes of more than of the first words.

Delvaux FIG. 6 shows an interleaver that stores bytes of an incoming sequence in a memory 120 and then reads the bytes out of the memory to produce an outgoing sequence that is a convolutionally interleaved version of the incoming sequence. One important difference between the interleaver shown by Delvaux and the apparatus recited in claim 1 is that Delvaux's interleaver uses only a single memory 120 rather than a main memory and a cache memory as recited in claim 1. In Delvaux's system, all of the words of the incoming sequence to be interleaved are stored in only memory 120 and all of the words of the interleaved outgoing sequence are read out directly out of that same memory 120. Thus Delvaux fails to teach the recited control circuit which can write bytes into either of two memories and that can transfer bytes between the two memories as recited in claim 1.

The Examiner cites Delvaux col. 3, lines 21-37 as teaching a main memory and cites col. 10 line 56-col. 11, line 27 as teaching a cache memory, however the two sections refer to the same memory. Although Delvaux's FIG. 6 shows only a single memory 120, it is divided into two sections, an interleave memory 122 and a "fast path" memory 124. However, the two memory sections 122 and 124 are not similar in purpose to the separate main and cache memories recited in claim 1. As Delvaux (col. 2,

lines 47-49 and col. 10, line 56 through col. 11, line 27) teaches, in addition to receiving a data sequence that is to be interleaved, the interleaver may also receive incoming words ("fast data") that are not part of any sequence to be interleaved. The "fast data" is simply received, stored and then forwarded in the same order without being convolutionally interleaved. Delvaux teaches that interleave memory section 122 is used only for storing only incoming data sequences to be interleaved while fast path memory section 124 is used for only for storing incoming fast data until it can be forwarded. Thus while Delvaux does show two memories (or memory sections) 122 and 124, there is no transfer of data between the two memories 122 and 124 as recited in claim 1. Thus, Claim 1 is patentable over Delvaux because Delvaux fails to teach the recited control circuit "for transferring bytes between the main memory and the cache memory" as recited in claim 1. Claims 2, 4 - 12, and 14-22 are patentable over Delvaux for similar reasons

Note that the apparatus recited in claim 1 can also be implemented by the applicant's deinterleaver of FIG. 7. Delvaux's FIG. 7 shows a deinterleaver 7 that includes two memories 222 and 224, however only memory 222 is used for storing data to be interleaved; memory 224 is used only for fast data, and there is no transfer of data between the two memories as recited in claim 1.

Claims 3 and 13

Claim 3 depends on claim 1 and is patentable over Delvaux for similar reasons.

Claim 3 further recites that the control circuit operates in a burst read or write mode when it read or write accesses sequential addresses in the main memory. Otherwise the control circuit independently read and write accesses individual address of the cache memory. In an interleaver or deinterleaver application, the applicant's control circuit independently read

and write accesses individual addresses of the cache memory because it has to build the outgoing sequence on a byte-by-byte basis from bytes that arrive out of order, but uses the burst mode to access the main memory because it is able to read and write byte sequences that arrive and depart in the same order. The ability to use the burst read and write access mode to access the main memory allows the applicant's interleaver/deinterleaver to use the relatively large but slow RAM to implement the main memory since burst mode access is relatively quick for reading and writing large blocks of data to an otherwise slow RAM.

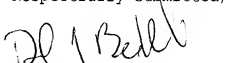
The Examiner cites various sections of Delvaux that mention the word "burst" but these sections of Delvaux relate to errors in data encoded into a signal sent through a data channel such as a pair of telephone wires that can occur as a result of "noise bursts". Delvaux does not discuss read or write accessing a memory in a "burst mode" as recited in claim 3. In the system described by Delvaux a data sequence representing speech such as a telephone conversation can be processed to reproduce the speech. If a burst of noise distorts a sufficiently large section of a signal representing a non-interleaved data sequence being transmitted over a telephone line, a section of the subsequently reproduced speech derived from that distorted signal section may be unintelligible. To avoid this, the data sequence is convolutionally interleaved before transmission to scramble its word order. After the sequence is received and deinterleaved to put the words back into proper order, the effects of a burst of noise that distort a section of the signal conveying interleaved sequence would be spread out over a wide portion of the reconstituted speech and would be less likely to cause any one section of the speech to be unintelligible.

Claim 3 is therefore further patentable over Delvaux because Delvaux does not teach to use the recited burst read mode or burst write mode when read or write accessing a main memory while independently accessing individual addresses of a separate

cache memory as recited in claim 3. Claim 13 is patentable over Delvaux for reasons generally similar to those expressed above in connection with claims 1 and 3.

6. In view of the foregoing amendments and remarks it is believed the application is in condition for allowance. Notice of Allowance is therefore respectfully requested.

Respectfully submitted,



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ABSTRACT

An apparatus for receiving and storing an incoming sequence and for forwarding the bytes of the incoming sequence as an outgoing sequence in a different byte order includes a cache memory and a main memory for storing bytes of the incoming sequence until they can be forwarded as bytes of the outgoing sequence. A control circuit selectively burst mode writes sequences of incoming bytes that need be stored for a relatively long time to blocks of sequential addresses of the main memory, writes individual bytes of the incoming sequence that need be stored for a relatively short time to selected addresses of the cache memory, and reads bytes out of the cache memory and the main memory when needed to form the outgoing sequence.